

009220-20052500

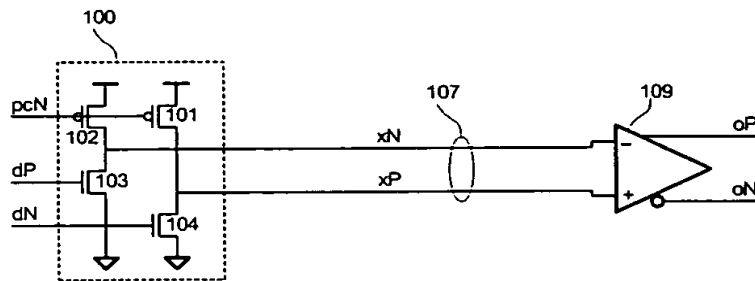


Figure 1: Prior Art

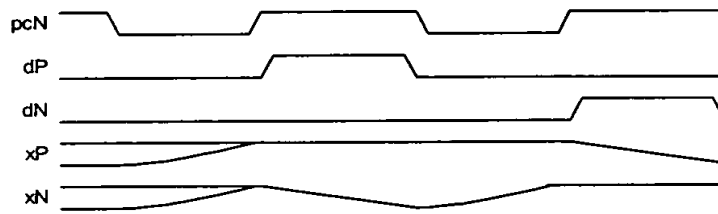


Figure 2: Prior Art

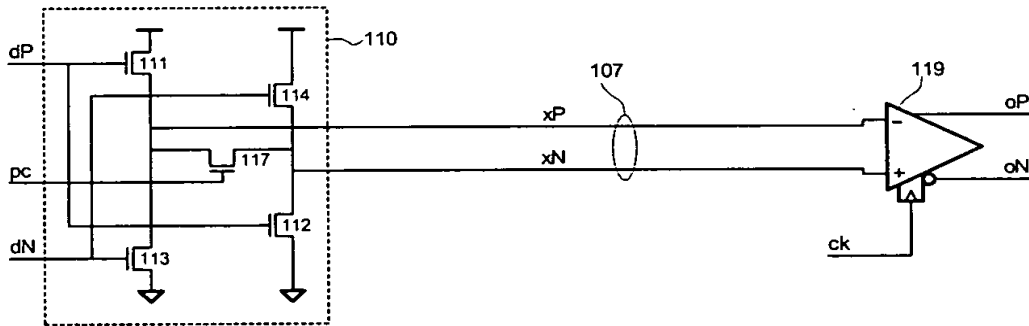


Figure 3

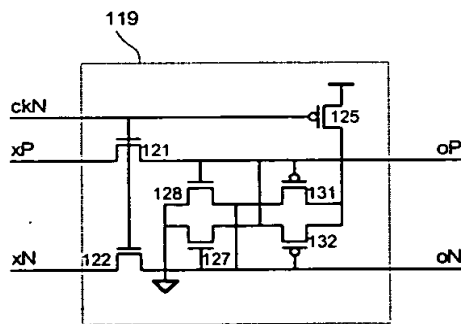


Figure 4

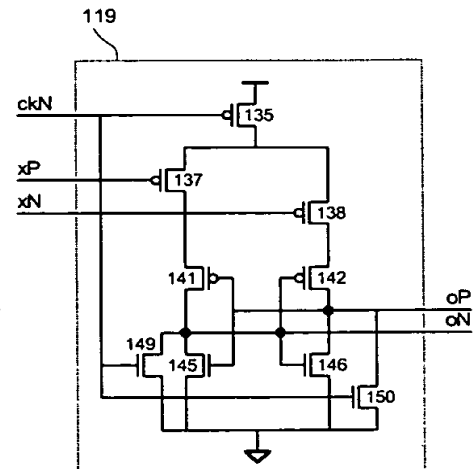


Figure 5



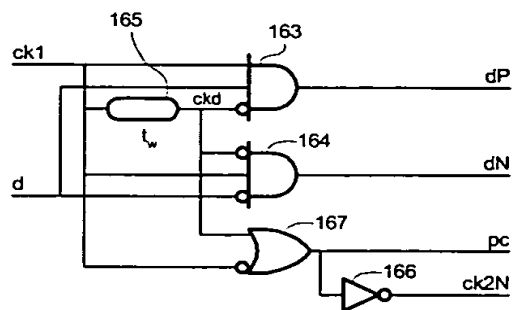


Figure 10

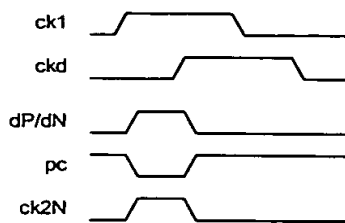


Figure 11

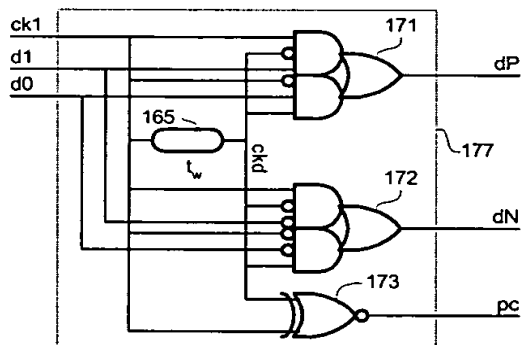


Figure 12

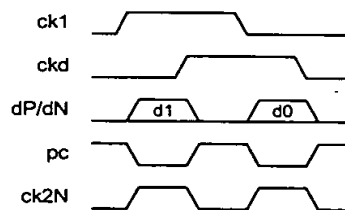


Figure 13

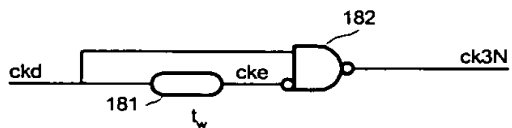


Figure 14

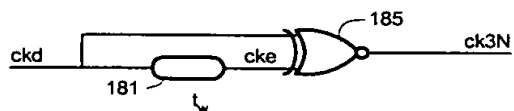


Figure 15

009220 20090930

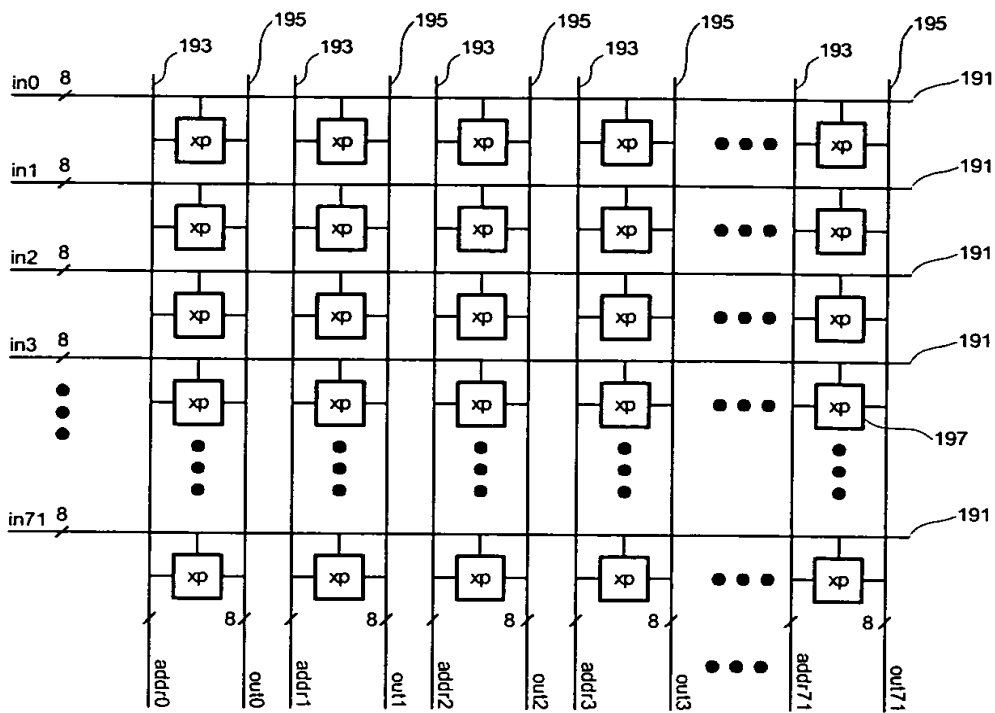


Figure 16

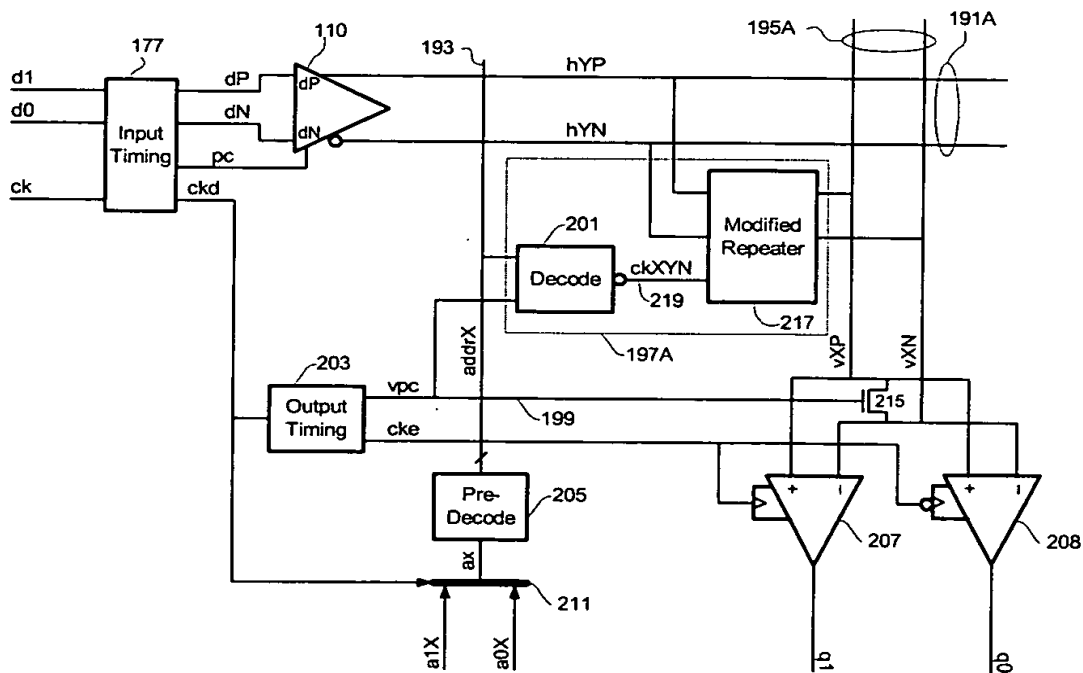


Figure 17

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The timing diagram shows the following signals and their waveforms:

- ck**: Clock signal, a periodic square wave.
- ckd**: Clock divider output, a square wave with a longer period than **ck**.
- cke**: Cache enable signal, a square wave that is active (low) during specific intervals.
- dP/dN**: Data bus signal, showing data **d1**, **d0**, and **d1'** being transferred.
- pc**: Program counter output, a square wave that is active (low) during specific intervals.
- hYP/hYN**: High-order address bus signal, showing address **a1**, **a0**, and **a1'** being transferred.
- addrX**: Address bus signal, showing address **a1**, **a0**, and **a1'** being transferred.
- vpc**: Valid program counter output, a square wave that is active (low) during specific intervals.
- ckXYN**: Cache control signal, a square wave that is active (low) during specific intervals.
- vXP/vXN**: Valid address bus signal, showing address **a1**, **a0**, and **a1'** being transferred.
- q1**: Cache control signal, a square wave that is active (low) during specific intervals.
- q0**: Cache control signal, a square wave that is active (low) during specific intervals.

Figure 18

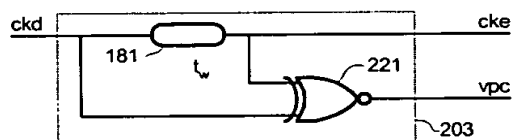


Figure 19

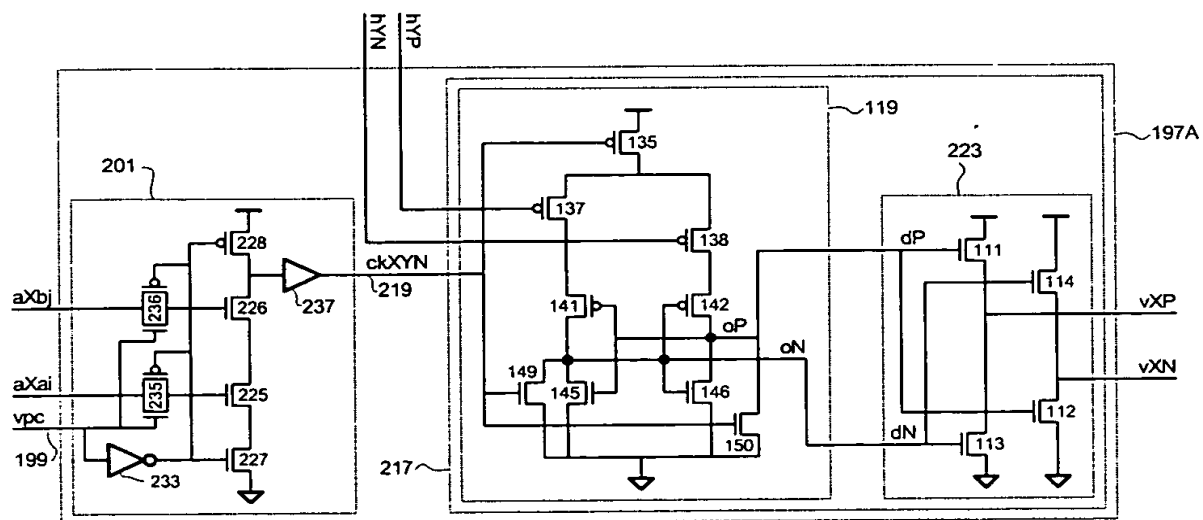


Figure 20

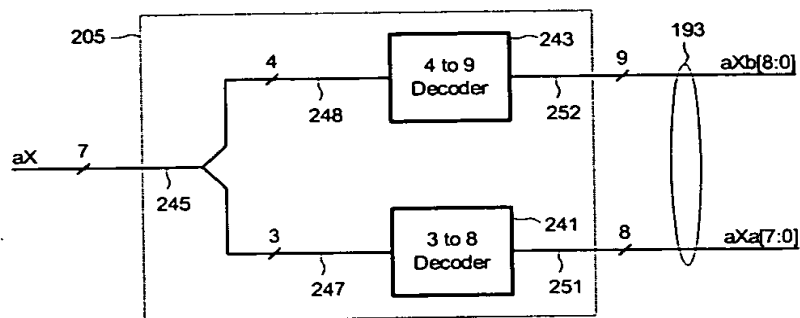


Figure 21

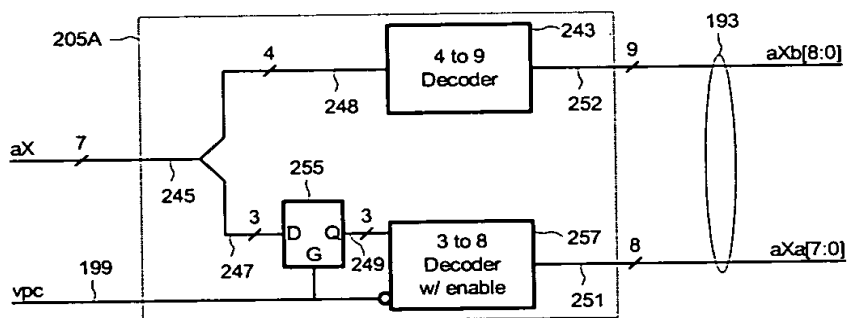


Figure 22

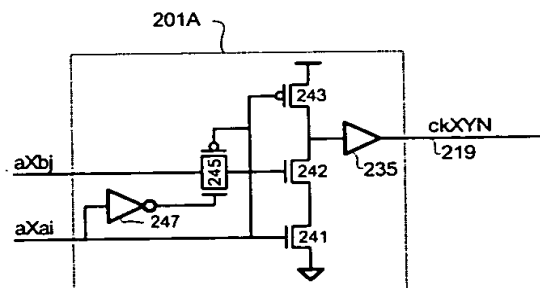


Figure 23

009220 20090900